REMARKS

The Office Action dated December 29, 2008, has been received and carefully noted. The above amendments and the following remarks are being submitted as a full and complete response thereto.

Claims 1-10 are currently pending and under examination. Claims 11-29 have been previously withdrawn from consideration. By the foregoing amendment, Claims 1, 5, 6, and 7 have been amended. Support for these amendments can be found in the specification as originally filed at, for example, Figs. 6-7 and their relative descriptions, such as steps 14-17 of Fig. 6, Thus, no new matter has been introduced.

In the Office Action, Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,757,763 to Preiss et al. ("Preiss") in view of U.S. Patent No. 5,898,848 to Gulick ("Gulick"). In response to Applicant's previous arguments, the Office Action asserts that it is the position of the office that providing target address information qualifies as communication control information so long as no data associated with the transfer information is stored in the same register. As for the newly added limitation of writing "data end information" at end of communication control information being written to the register, the Office Action asserts that it would be obvious to one of ordinary skill that frame entries tend to include end of data/packet bit to indicate the completion of frame data.

It is noted that Claims 1, 5, 6, and 7 have been amended. To the extent that the grounds for rejection are still applicable to the currently pending claims, they are respectfully traversed.

Claim 1, as amended, recites, among other things, a status register storing information indicating a status of the receive buffer, the receive register, the transmit buffer, and the transmit register, the status indicating that the receive buffer is full of data, the transmit buffer is full of data, new information has been written in the receive register, and new information has been written in the treatment register, and a control circuit for passing the communication data stored in said buffer to a second device connected to the second bus, and passing the data end information stored in said register to the second device, wherein the communication control information and the communication data are sent via the register and the buffer, respectively, and the second device reads out data stored in the buffer if the status register indicates that the buffer is full of data, and that new information has been written in the register, and performs an appropriate receive process according to the control information and completes the receive process when detecting the data end information.

Claim 6, as amended, recites a status register storing information indicating a status of the first buffer, the first register, the second buffer, and the second register, the status indicating that the first buffer is full of data, the second buffer is full of data, new information has been written in the first register, and new information has been written in the second register, and a control circuit passing the first communication data stored in said first buffer to the second device and the first data end information stored in said first register to the second device, and further passing the second communication data stored in said second buffer to the first device and the second data end information stored in said second register to the first device, wherein the first and second communication control information are sent via the first and second registers,

respectively, and the first and second communication data are sent via the first and second buffers, respectively, the first device reads out data stored in the second buffer if the status register indicates that the second register is full of data and that new information has been written in the second register, the second device reads out data stored in the first buffer if the status register indicates that the first buffer is full of data, and that new information has been written in the first register, and the first device and the second device, and the first device and the second device perform an appropriate receive process according to the second and first control information, respectively, and complete the receive process when detecting the data end information.

Claim 7, as amended, recites a status register storing information indicating a status of the receive buffer, the receive register, the transmit buffer, and the transmit register, the status indicating that the receive buffer is full of data, the transmit buffer is full of data, new information has been written in the receive register, and new information has been written in the treatment register, and a control circuit for passing the receive data stored in said receive buffer to said internal CPU and passing the receive communication control information stored in said receive register to said internal CPU, and further passing the transmit data stored in said transmit buffer to said external host apparatus and passing the transmit communication control information stored in said transmit register to said external host apparatus, wherein the receive data and receive communication control information are sent via the receive buffer and receive register, respectively, and the transmit data and transmit communication control information are sent via the transmit buffer and transmit register, respectively, and wherein said internal CPU reads out data stored in the receive buffer if the status

register indicates that the receive buffer is full of data and if the status register indicated that new information has been written in the receive register, said external host apparatus reads out data stored in the transmit buffer if the status register indicates that the transmit buffer is full of data, and that new information has been in the transmit register, and said internal CPU and said external host apparatus perform an appropriate process according to the control information and complete the process when detecting the data end information.

The Office Action asserts that it would have been obvious to one of ordinary skill in the art to combine Preiss and Gulick in order to provide a more efficient bus bridge interconnect architecture for multimedia-related devices for interconnection and for interfacing to a standard bus. Applicants respectfully disagree. As admitted in the previous Office Action, Preiss fails to disclose storing the communication control information in a register and transferring the communication data (stored in the buffer) in addition to the communication control information (stored in the register) to the designation device.

It is submitted that Gulick merely discloses, in a data transfer process, transferring data and communication control information, which is different from the data such as a target address, via different routes. However, Gulick fails to disclose or suggest a status register which indicates a status of a buffer used for transferring data and a status of a register used for transferring communication control information.

By contrast, claim 1 claims that a status register indicates that the status of the buffer and the status of the register, and a receiving-side device performs an appropriate receive process based on the status indicated by the status register. When the status

register indicates a buffer full status, data is transferred from the buffer. The communication control information is referred only when the status register indicates that new information has been written in the register.

Accordingly, neither Preiss nor Gulick, alone or combined, discloses or suggests at least the features of Claims 1, 6, and 7, as stated above. For at least this reason, Applicants submit that Claims 1, 6, and 7 are allowable over the applied art of record. As Claims 1 and 7 are allowable, Claims 2-5 and 8-10, which depend from allowable Claims 1 and 7, respectively, are likewise allowable for at least the reasons set forth above with respect to Claims 1 and 7.

Conclusion

For all of the above reasons, it is respectfully submitted that claims 1-10 are in condition for allowance and a Notice of Allowability is earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is invited to contact the undersigned representative at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The Commissioner is hereby authorized to

charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300 referencing client matter number **107337-00106**.

Respectfully submitted,
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